WE CLAIM:

1. A metal structure for a contact pad of an integrated circuit having copper interconnecting metallization protected by an overcoat, comprising:

   a portion of said copper metallization exposed by a window in said overcoat;

   said exposed copper having a clean surface;

   a patterned copper layer directly positioned on said clean copper metallization, whereby said metal structure has an electrical conductivity about equal to the conductivity of pure copper, said layer overlapping the perimeter of said overcoat window; and

   a copper stud positioned on said copper layer, following the contours of said copper layer.

2. The metal structure according to Claim 1 wherein said clean copper surface is free of copper oxide, organic residues, and contamination.

3. The metal structure according to Claim 1 wherein said direct positioning of said copper layer on said clean copper pad provides the lowest possible electrical resistance and relinquishes the need for an intermediate barrier or under-bump layer.

4. The metal structure according to Claim 1 wherein said copper layer has a thickness in the range from about 0.3 to 0.8 μm.

5. The metal structure according to Claim 1 wherein said overcoat is a moisture-impermeable inorganic layer including silicon nitride and silicon oxynitride of approximately 1.0 μm thickness.

6. The metal structure according to Claim 5 wherein said

inorganic layer forms a perimeter around said window having a slope coverable by said copper layer.

7. The metal structure according to Claim 1 wherein said overcoat is a sequence of an inorganic layer adjacent to the integrated circuit, overlaid by a polymeric layer including polyimide, benzocylobutene, and polybenzoxazole of approximately 3.0 to 10.0 μm thickness, capable of absorbing thermomechanical stress.

8. The metal structure according to Claim 7 wherein said sequence of layers forms a perimeter around said window having a slope coverable by said copper layer.

9. The metal structure according to Claim 1 wherein said copper layer follows the contour of said perimeter of said overcoat window.

10. The metal structure according to Claim 1 wherein said copper stud has a thickness in the range from about 10 to 20 μm and a width equal to the extent of said copper layer, following the contour of said perimeter of said overcoat window.

11. A structure for metallurgical connections between solder bumps and contact pads positioned on integrated circuits having copper interconnecting metallization protected by an overcoat, comprising:

a portion of said copper metallization exposed by a window in said overcoat;

said exposed copper having a clean surface;

a patterned copper layer directly positioned on said clean copper metallization, whereby said metal structure has an electrical conductivity about equal to the conductivity of pure copper, said layer overlapping the perimeter of said overcoat

window;

a copper stud positioned on said copper layer; and

one of said solder bumps bonded to said copper stud.

12. The structure according to Claim 11 wherein said solder bumps are selected from a group consisting of tin, indium, tin/lead, tin/indium, tin/silver, tin/bismuth, conductive adhesives, and z-axis conductive materials.

13. A wafer-level method for cleaning the surface of copper metallization used as integrated circuit interconnection and exposed in contact pads, comprising the steps of:

exposing said wafer to organic solvents, thereby removing organic contamination and mechanical particles from said copper contact pads, and drying said wafer;

exposing said wafer to an oxygen and nitrogen/argon/helium plasma, thereby ashing any organic residue on said copper contact pads and oxidizing said copper surface to a controlled thickness of less than 10 nm;

without breaking the vacuum, exposing said wafer to a first hydrogen and nitrogen/helium/argon plasma, thereby removing said controlled copper oxide from said pad surface and passivating said cleaned surface;

sputter-etching said passivated pad surface with energetic ions, thereby creating a fresh surface and concurrently activating it;

sputter-depositing a layer of copper covering said fresh pad surface and pad perimeter, said layer providing minimal electrical resistance and thermo-mechanical stress to said pad;

exposing said wafer to a second hydrogen and nitrogen/argon plasma, thereby passivating said copper layer; and

without exposing said passivated copper layer to fresh contamination, depositing a copper stud onto said copper layer.

14. The method according to Claim 13 further comprising the process step of depositing a solder bump onto said copper stud.

15. The method according to Claim 13 wherein said process step of depositing a copper stud is selected from a group of processes consisting of:

electroplating said copper stud onto said copper layer, thereby enabling an electroplating process for depositing said solder bump, providing small pitch center-to-center bumps; and

electroless plating said copper stud onto said copper layer, thereby enabling a screen-printing process for depositing said solder bump, or an attachment process of pre-fabricated solder balls, providing large pitch center-to-center balls.

16. The method according to Claim 13 wherein said process step of exposing the wafer to solvents is selected from a group of processes consisting of:

submerging said wafer in agitated isopropyl alcohol, methanol, glycol, N-methyl pyrrolidone and other solvents;

adding ultrasonic energy to said solvent;

spraying said wafer with an organic solvent; and

treating said wafer in dry chemical vapor.

17. The method according to Claim 13 further comprising,

between said steps of oxygen plasma and nydrogen plasma, the step of etching in an aqueous inorganic or organic acid, thereby removing deep copper pad defects.

18. The method according to Claim 13 wherein said step of sputter-depositing a layer of copper is performed without breaking the vacuum after said step of first hydrogen plasma cleaning, thereby omitting the second wet and hydrogen-based cleanings.